REMARKS

The Final Office Action mailed March 14, 2007, has been received and reviewed. Claims 1, 3-22, 24-27, 31-40, 42 and 43 are currently pending in the application. Claims 1, 3-22, 24-27, 31-40, 42 and 43 stand rejected. Applicants propose to amend claims 1, 7, 9, 12, 14, 18, 21, 24, 25, 26, 31, 35, 38, 42 and 43. No new matter is added. Reconsideration is respectfully requested.

Information Disclosure Statement

Please note that an Information Disclosure Statement was filed herein on December 6, 1999, and that no copy of the PTO-1449 was returned with the outstanding Office Action. It is respectfully requested that an initialed copy of the PTO-1449 evidencing consideration of the cited references be returned to the undersigned attorney.

35 U.S.C. § 112 Claim Rejections

Claims 9, 10, 12, 13 and 21 stand rejected under 35 U.S.C. § 112, first paragraph, as containing subject matter which was not described in the specification in such a way as to reasonably convey to one skilled in the relevant art that the inventor(s), at the time the application was filed, had possession of the claimed invention. Applicants respectfully traverse this rejection, as hereinafter set forth.

Claims 9, 10, 12 and 13 stand rejected under 35 U.S.C. § 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicants regard as the invention. Applicants respectfully traverse this rejection, as hereinafter set forth.

Claim 9 has been amended to recite "The method according to Claim 7, wherein planarizing the conformal layer comprises using an etch recipe that etches the conformal layer faster than the first dielectric layer by a ratio in a range from about 1:1 to about 2:1." Claim 12 has been similarly amended. "Support for the amendment may be found throughout the as-filed specification including, for example page 14, lines 14-21. Reconsideration and withdrawal of the rejection is requested.

Claim 21 has been amended to recite "wherein rounding the top edges of each of the isolation trenches comprises forming a liner upon a sidewall of each isolation trench, the liner being confined preferentially within each isolation trench and extending from an interface thereof with the oxide layer to the termination of the isolation trench within the semiconductor substrate, and wherein the conformal third layer is composed of an electrically insulative material." Support for the amendment may be found throughout the as-filed specification including, for example, page 12, lines 1-13. wherein rounding the top edges of each of the isolation trenches comprises forming a liner upon a sidewall of each isolation trench, the liner being confined preferentially within each isolation trench and extending from an interface thereof with the oxide layer to the termination of the isolation trench within the semiconductor substrate, and wherein the conformal third layer is composed of an electrically insulative material.

35 U.S.C. § 102(e) Anticipation Rejections

Anticipation Rejection Based on U.S. Patent No. 6,097,072 to Omid-Zahoor et al.

Claim 38 stands rejected under 35 U.S.C. § 102(e) as being anticipated by Omid-Zahoor et al. (U.S. Patent No. 6,097,072). Applicants respectfully traverse this rejection, as hereinafter set forth.

A claim is anticipated only if each and every element as set forth in the claim is found, either expressly or inherently described, in a single prior art reference. *Verdegaal Brothers v. Union Oil Co. of California*, 2 USPQ2d 1051, 1053 (Fed. Cir. 1987). The identical invention must be shown in as complete detail as is contained in the claim. *Richardson v. Suzuki Motor Co.*, 9 USPQ2d 1913, 1920 (Fed. Cir. 1989).

Omid-Zohoor discloses a method of forming trenches with suppressed parasitic edge transistors. Trenches 360 are formed in a substrate 120 having a pad oxide layer 340 and silicon nitride layer 344 thereon. (Omid-Zohoor, FIG. 3I). Spacers 356 may flank the trenches 360. A thick oxide layer 364 is deposited to cover the wafer and fill the trenches 360. A reverse mask 368 is placed over defined trench regions. The mask is followed by an etch which creates oxide

ridges . (Omid-Zohoor, col. 4, lines 47-55, FIG. 3L). The upper surface of the oxide layer 372 is polished to expose the silicon nitride layer 344. (*Id.,* FIG. 3M).

Claim 38 of the presently claimed invention recites "A method for forming a microelectronic structure, the method comprising: providing a semiconductor substrate having a top surface with an oxide layer thereon; forming a first layer upon the oxide layer; selectively removing the first layer to expose the oxide layer at a plurality of areas; forming a plurality of isolation trenches through the oxide layer at the plurality of areas, wherein an electrically insulative material extends continuously between and within the plurality of isolation trenches without filling the plurality of isolation trenches, each isolation trench: having a spacer composed of a dielectric material upon the oxide layer in contact with the first layer; extending from an opening thereto at the top surface of the semiconductor substrate and below the oxide layer into and terminating within the semiconductor substrate adjacent to and below the spacer; having a second layer filling the isolation trench and extending above the oxide layer in contact with the spacer, wherein the filling is performed by depositing the second layer, and the depositing is carried out to the extent of filling each isolation trench and extending over the spacer and over the first layer so as to define an upper surface contour of the second layer; and having a planar upper surface formed from the second layer and the spacer and being situated above the oxide layer, wherein the planar upper surface is formed by substantially simultaneously subjecting the entire upper surface contour of the second layer to a planarizing process; and fusing the oxide layer, electrically insulative material, spacer and second layer, wherein the microelectronic structure is defined at least in part by the plurality of spacers, the second layer, and the plurality of isolation trenches." Support for the amendment may be found throughout the as-filed specification including, for example, page 12, lines 1-24 and FIGs. 5A/B and related text, and page 15, lines 18-22.

By way of contrast with claim 38, Omid-Zohoor teaches oxide layer 364 filling trenches 360 and extending over the upper surface of semiconductor substrate 120. (Omid-Zohoor, FIG. 3J). Accordingly, Omid-Zohoor fails to disclose, either expressly or inherently, "forming a plurality of isolation trenches through the oxide layer at the plurality of areas, wherein an electrically insulative material extends continuously between and within the plurality of isolation

trenches without filling the plurality of isolation trenches" as recited in claim 38 of the presently claimed invention.

Omid-Zohoor also teaches the planarizing of the reduced oxide layer 372 with oxide ridges 373 until silicon nitride layer 344 is exposed (Omid-Zohoor, FIGs. 3L and 3M, col. 4, lines 54-57, 59-61) and does not teach "substantially simultaneously subjecting the entire upper surface contour of the second layer to a planarizing process" as recited by claim 38 as the planarization is conducted on a layer that had part of the conformal layer removed along with the reverse-resist mask. Therefore, the planarization is not conducted on a layer having the upper surface contour created by the deposition of the conformal layer. As such, Omid-Zohoor does not teach or suggest planarizing the entire upper surface contour created by the deposition of the conformal layer.

Additionally, Omid-Zohoor fails to disclose "fusing the oxide layer, electrically insulative material, spacer and second layer" as recited in claim 38. As Omid-Zohoor fails to disclose, either expressly or inherently, every element of claim 38 of the presently claimed invention, it cannot anticipate claim 38. Reconsideration and withdrawal of the rejection is requested.

35 U.S.C. § 103(a) Obviousness Rejections

Obviousness Rejection Based on U.S. Patent No. 6,097,072 to Omid-Zohoor in view of U.S. Patent No. 5,387,540 to Poon et al.

Claims 1, 3-22, 24-26, and 31-34 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Omid-Zohoor (U.S. Patent 6,097,072) in view of Poon (U.S. Patent 5,387,540). Applicants respectfully traverse this rejection, as hereinafter set forth.

M.P.E.P. 706.02(j) sets forth the standard for a Section 103(a) rejection:

> To establish a *prima facie* case of obviousness, three basic criteria must be met. First, there must be some suggestion or motivation, either in the references themselves or in the knowledge generally available to one of ordinary skill in the art, to modify the reference or combine reference teachings. Second, there must be a reasonable expectation of success. Finally, **the prior art reference (or references when combined) must teach or suggest all the claim limitations.** The teaching or suggestion to make the claimed combination and the reasonable expectation of success must both be found in the prior art, and not based on

applicant's disclosure. *In re Vaeck*, 947 F.2d 488, 20 USPQ2d 1438 (Fed. Cir. 1991). (Emphasis added).

The discussion of Omid-Zohoor is incorporated herein. Poon is cited for teaching the formation of a thermal liner within a trench surface. Applicants respectfully submit the proposed combination of references fail to teach or suggest every element of the presently claimed invention.

Claim 1 avoids the combination of Omid-Zohoor and Poon. By way of contrast with the cited art, claim 1 of the presently claimed invention recites, in part, "filling each isolation trench with a conformal layer. . . so as to define an upper surface contour of the conformal layer," "substantially simultaneously subjecting the entire upper surface contour of the conformal layer to a planarizing process and planarizing the conformal layer at least to the first dielectric layer and each spacer to form therefrom an upper surface for each isolation trench that is co-planar to the other upper surfaces" and fusing the oxide layer, liner, spacers and conformal layer." Support for the amendment may be found throughout the as-filed specification including, for example, page 15, lines 18-22.

By contrast, Omid-Zohoor teaches the deposition of a reverse-resist mask 368 over trench regions 356 (Omid-Zohoor, FIG. 3K, col. 4, lines 51-52) and subsequent wet or dry etch to partially remove oxide layer 364 and leave a reduced oxide layer 372 with ridges 373 (*Id.*, FIG. 3L, col. 4, lines 52-54). Applicants respectfully submit that Omid-Zohoor does not teach or suggest all of the limitations of claim 1 as the presence of the reverse-resist mask protects a portion of the conformal layer and thus prevents "substantially simultaneously subjecting the entire upper surface contour of the conformal layer to a planarizing process and planarizing the conformal" as recited in claim 1.

Applicants further submit that the planarizing of the reduced oxide layer 372 with oxide ridges 373 until silicon nitride layer 344 is exposed (Omid-Zohoor, FIGs. 3L and 3M, col. 4, lines 54-57, 59-61) also does not teach or suggest this limitation as the planarization is conducted on a layer that had part of the conformal layer removed along with the reverse-resist mask.

Therefore, Omid-Zohoor does not teach or suggest planarizing the entire upper surface contour created by the deposition of the conformal layer.

Additionally, Omid-Zohoor fails to teach or suggest "fusing the oxide layer, liner, spacers and conformal layer" as recited in claim 1.

Since Poon is relied on for teaching forming a thermal liner within a trench surface, Poon fails to cure the deficiencies of Omid-Zohoor. As the proposed combination of references fails to teach or suggest all of the limitations of the presently claimed invention, Applicants respectfully submit that Omid-Zohoor in view of Poon does not render claim 1 obvious. Accordingly, claim 1 is allowable.

Claims 3-6 are each allowable, at least for the same reasons as allowable claim 1.

Each of independent claims 7, 14, 18, 24, 25, 26, and 31 has been amended to be substantially similar to claim 1 in regard to the limitations of "filling each isolation trench with a conformal layer. . . so as to define an upper surface contour of the conformal layer," "substantially simultaneously subjecting the entire upper surface contour of the conformal layer to a planarizing process and planarizing the conformal" and "fusing the oxide layer, liner, spacers and conformal layer." As such, applicants respectfully submit that each of independent claims 7, 14, 18, 24, 25, 26, and 31 is allowable at least for substantially the same reasons as independent claim 1.

Applicants respectfully submit that dependent claims 8-13, 15-17, 19-22, and 32-34 are at least allowable as depending from an allowable independent claim

Claim 9 is further allowable as the cited references fail to teach or suggest that planarizing the conformal layer comprises using an etch recipe that etches the conformal layer faster than the first dielectric layer by a ratio in a range from about 1:1 to about 2:1.

Claim 12 is further allowable because the cited references do not teach or suggest that the upper surface for each of the isolation trenches is formed in an etch process using an etch recipe that etches the conformal layer faster than the first dielectric layer by a ratio in a range from about 1:1 to about 2:1.

Claims 10 and 13 are further allowable because the cited references do not teach or suggest that the ratio is in a range from about 1.3:1 to about 1.7:1.

For the foregoing reasons, applicants respectfully request the withdrawal of the rejections of claims 1, 3-22, 24-26, and 31-34 under 35 U.S.C. § 103(a) and reconsideration of same.

Obviousness Rejection Based on U.S. Patent No. 6,097,072 to Omid-Zohoor and U.S. Patent No. 5,387,540 to Poon in view of U.S. Patent No. 6,069,083 to Miyashita et al.

Claim 27 stands rejected under 35 U.S.C. § 103(a) as being unpatentable over Omid-Zohoor (U.S. Patent No. 6,097,072) and Poon (U.S. Patent No. 5,387,540) as applied to claim 26 above, and further in view of Miyashita et al. (U.S. Patent No. 6,069,083). Applicants respectfully traverse this rejection, as hereinafter set forth.

Miyashita is cited for allegedly teaching "planarizing the conformal layer in a single-step by an etch using an etch recipe that etches the conformal layer faster than the first dielectric layer by a ratio from about 1 to about 3." Miyashita fails to cure the deficiencies of Omid-Zohoor and Poon.

The Court of Appeals for the Federal Circuit has stated that "dependent claims are nonobvious under section 103 if the independent claims from which they depend are nonobvious." In re Fine, 5 USPQ2d 1596, 1600 (Fed. Cir. 1988). See also MPEP § 2143.03. Having failed to teach or suggest each and every limitation of the current application, the prior art referenced as rendering dependent claim 27 obvious, cannot serve as a basis for rejection.

Obviousness Rejection Based on U.S. Patent No. 6,097,072 to Omid-Zohoor

Claim 35 stands rejected under 35 U.S.C. § 103(a) as being unpatentable over Omid-Zohoor (U.S. Patent No. 6,097,072). Applicants respectfully traverse this rejection, as hereinafter set forth.

The discussion of Omid-Zohoor is incorporated herein.

Independent claim 35, as amended, recites, in part, "having a second layer filling the isolation trench . . . so as to define an upper surface contour of the second layer," "substantially simultaneously subjecting the entire upper surface contour of the second layer to a planarizing process" and "fusing the oxide layer, spacer and second layer." Support for the amendment may be found throughout the as-filed specification including, for example, page 15, lines 18-22.

As discussed, Omid-Zohoor teaches the deposition of a reverse-resist mask 368 over trench regions 356 (Omid-Zohoor, FIG. 3K, col. 4, lines 51-52) and subsequent wet or dry etch to partially remove oxide layer 364 and leave a reduced oxide layer 372 with ridges 373 (*Id.*, FIG. 3L, col. 4, lines 52-54). Applicants respectfully submit that Omid-Zohoor does not teach or suggest all of the limitations of claim 35, as amended, as the presence of the reverse-resist mask protects a portion of the conformal layer and thus prevents "substantially simultaneously subjecting the entire upper surface contour of the conformal layer to a planarizing process" as recited in claim 35.

Applicants further submit that the planarizing of the reduced oxide layer 372 with oxide ridges 373 until silicon nitride layer 344 is exposed (Omid-Zohoor, FIGs. 3L and 3M, col. 4, lines 54-57, 59-61) also does not teach "substantially simultaneously subjecting the entire upper surface contour of the second layer to a planarizing process" as recited by claim 35 as the planarization is conducted on a layer that had part of the conformal layer removed along with the reverse-resist mask. Therefore, the planarization is not conducted on a layer having the upper surface contour created by the deposition of the conformal layer. As such, Omid-Zohoor does not teach or suggest planarizing the entire upper surface contour created by the deposition of the conformal layer.

Additionally, Omid-Zohoor fails to teach or suggest "fusing the oxide layer, spacer and second layer." As Omid-Zohoor fails to teach or suggest all of the limitations of the presently claimed invention, Applicants respectfully submit Omid-Zohoor does not render claim 35 of the presently claimed invention obvious. Accordingly, claim 35 is allowable. Reconsideration and withdrawal of the rejection is requested.

Obviousness Rejection Based on U.S. Patent No. 6,097,072 to Omid-Zohoor in view of Wolf Silicon Processing for the VLSI Era, Vol. 2, pp. 54 and 55

Claims 36-37, 39-40 and 42-43 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Omid-Zohoor (U.S. Patent No. 6,097,072) in view of Wolf Silicon Processing for the VLSI Era, Vol. 2, pp. 54 and 55. Applicants respectfully traverse this rejection, as hereinafter set forth.

The discussion of Omid-Zohoor is incorporated herein. Wolf is cited for teaching that the top edge of an isolation trench may be rounded and that the semiconductor substrate may be doped. Wolf fails to cure the deficiencies of Omid-Zohoor. Applicants respectfully submit the proposed combination of references fails to teach or suggest all of the limitations of the presently claimed invention

The Court of Appeals for the Federal Circuit has stated that "dependent claims are nonobvious under section 103 if the independent claims from which they depend are nonobvious." In re Fine, 5 USPQ2d 1596, 1600 (Fed. Cir. 1988). See also MPEP § 2143.03. Having failed to teach or suggest each and every limitation of the current application, the prior art referenced as rendering dependent claims 36 and 37 obvious, cannot serve as a basis for rejection.

Independent claim 38, as amended, recites, in part, "having a second layer filling the isolation trench . . . so as to define an upper surface contour of the second layer," "substantially simultaneously subjecting the entire upper surface contour of the second layer to a planarizing process" and "fusing the oxide layer, electrically insulative material, spacer and second layer." Support for the amendment may be found throughout the as-filed specification including, for example, page 15, lines 18-22.

As discussed, Omid-Zohoor teaches the deposition of a reverse-resist mask 368 over trench regions 356 (Omid-Zohoor, FIG. 3K, col. 4, lines 51-52) and subsequent wet or dry etch to partially remove oxide layer 364 and leave a reduced oxide layer 372 with ridges 373 (*Id.*, FIG. 3L, col. 4, lines 52-54). Applicants respectfully submit that Omid-Zohoor does not teach or suggest all of the limitations of claim 38 of the presently claimed invention as the presence of the reverse-resist mask protects a portion of the conformal layer and thus prevents "substantially simultaneously subjecting the entire upper surface contour of the conformal layer to a planarizing process" as recited in claim 38.

Applicants further submit that the planarizing of the reduced oxide layer 372 with oxide ridges 373 until silicon nitride layer 344 is exposed (Omid-Zohoor, FIGs. 3L and 3M, col. 4, lines 54-57, 59-61) also does not teach "substantially simultaneously subjecting the entire upper surface contour of the second layer to a planarizing process" as recited by claim 35 as the

planarization is conducted on a layer that had part of the conformal layer removed along with the reverse-resist mask. Therefore, the planarization is not conducted on a layer having the upper surface contour created by the deposition of the conformal layer. As such, Omid-Zohoor does not teach or suggest planarizing the entire upper surface contour created by the deposition of the conformal layer.

Additionally, Omid-Zohoor fails to teach or suggest "fusing the oxide layer, electrically insulative material, spacer and second layer."

Since Wolf is relied upon for teaching that a top edge of an isolation trench may be rounded and that the semiconductor substrate may be doped, Wolf fails to cure the deficiencies of Omid-Zohoor. As the proposed combination of references fails to teach or suggest all of the limitations of the presently claimed invention, Applicants respectfully submit Omid-Zohoor in view of Wolf does not render claim 38 of the presently claimed invention obvious. Accordingly, claim 38 is allowable.

Applicants respectfully submit that dependent claims 39 and 40 are at least allowable as depending from allowable independent claim 38.

Independent claims 42, and 43 have been amended to be substantially similar to claim 38 in regard to the limitations of "a conformal second layer" . . . filling each of the isolation trenches . . . so as to define an upper surface contour of the conformal second layer," "substantially simultaneously subjecting the entire upper surface contour of the second layer to a planarizing process" and "fusing the oxide layer, first spacer, second spacer and conformal second layer of the first isolation structure and fusing the oxide layer, first spacer, second spacer and conformal second layer of the second isolation structure." As such, applicants respectfully submit that independent claims 42 and 43 are allowable at least for substantially the same reasons as independent claim 38.

In view of the foregoing, applicants respectfully request that the rejection of claims 36-40, 42, and 43 under 35 U.S.C. § 103 be withdrawn.

ENTRY OF AMENDMENTS

The proposed amendments to the claims above should be entered by the Examiner because the amendments are supported by the as-filed specification and drawings and do not add any new matter to the application. Further, the amendments do not raise new issues or require a further search. Finally, if the Examiner determines that the amendments do not place the application in condition for allowance, entry is respectfully requested upon filing of a Notice of Appeal herein.

CONCLUSION

Claims 1, 3-22, 24-27, 31-40, 42, and 43 are believed to be in condition for allowance, and an early notice thereof is respectfully solicited. Should the Office determine that additional issues remain which might be resolved by a telephone conference, the Examiner is respectfully invited to contact Applicants' undersigned attorney.

Respectfully submitted,

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